ORIGINALLY SUBMITTED INFORMAL DRAWINGS
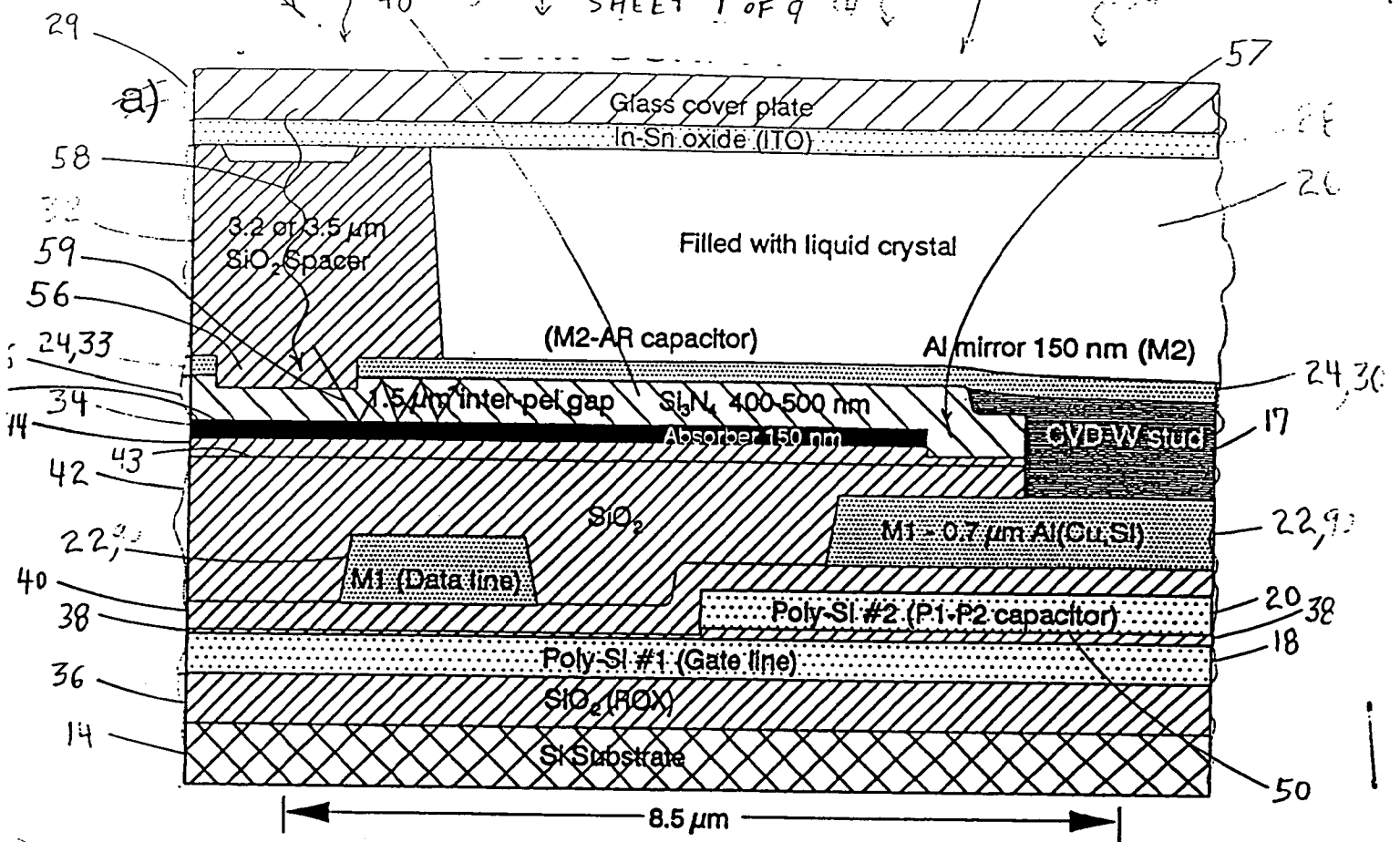
a)
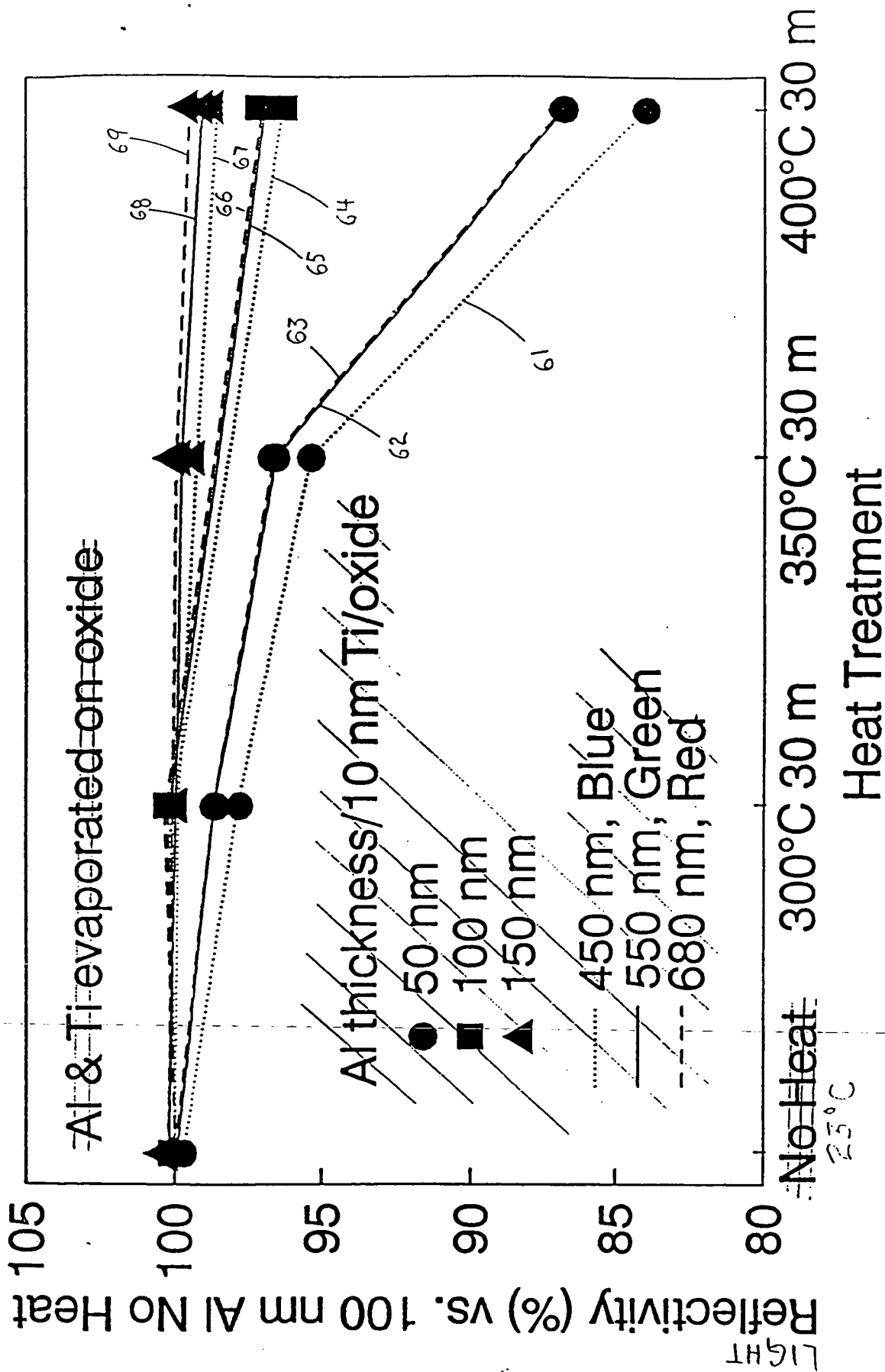
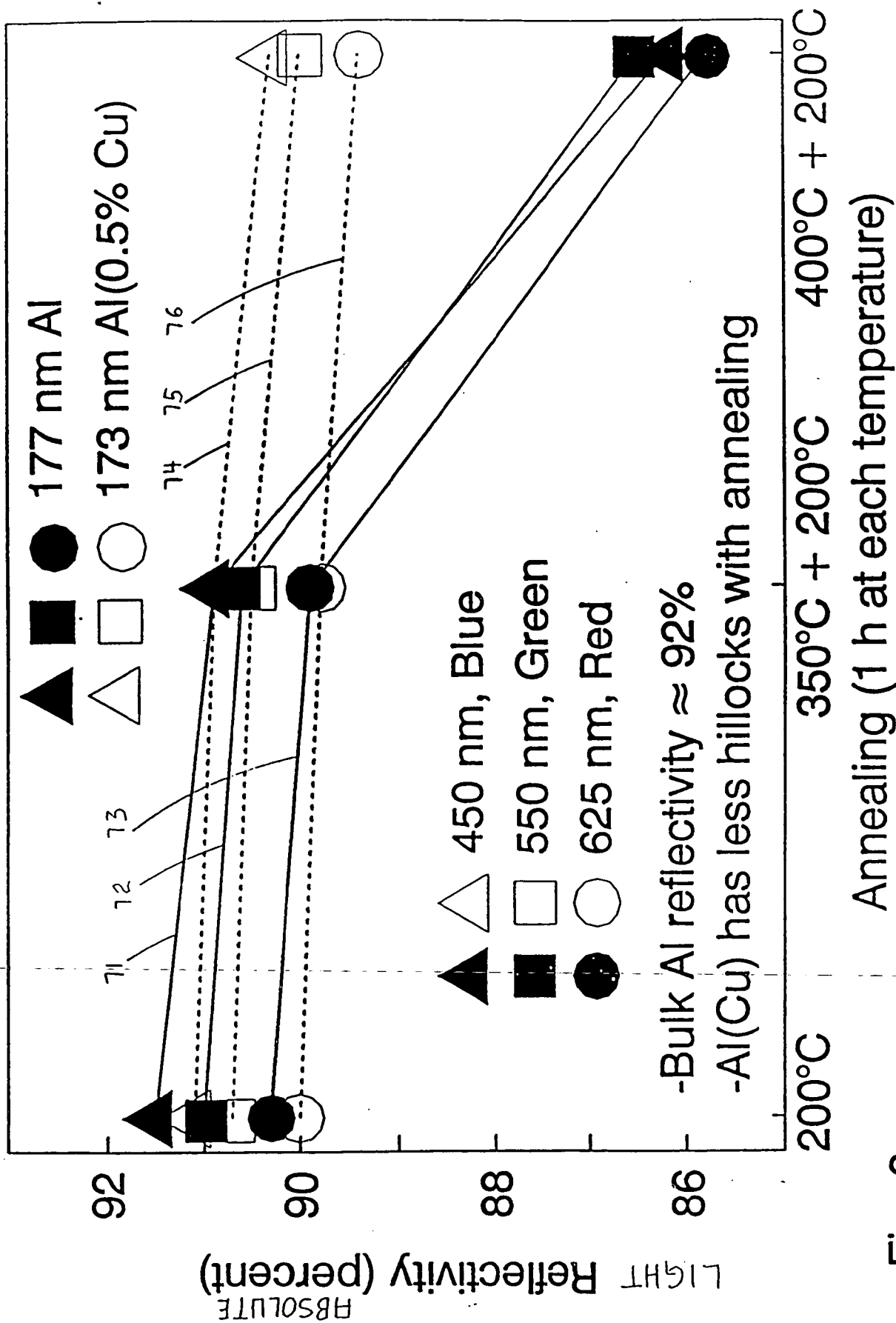Glass cover plate

In-Sn oxide (ITO)

3.2 or 3.5 μm SiO₂ Spacer

Filled with liquid crystal

(M2-AR capacitor)

Al mirror 150 nm (M2)

1.5 μm inter-pel gap   Si₃N₄ 400-500 nm

Absorber 150 nm

SiO₂

CVD W stud

M1 (Data line)

M1 - 0.7 μm Al(CuSi)

Poly-Si #2 (P1-P2 capacitor)

Poly-Si #1 (Gate line)

SiO₂ (ROX)

Si Substrate

← 8.5 μm →

FIG 1

Fig. 2

Fig. 3

Legend:

177 nm Al — ● ■ ▲
173 nm Al(0.5% Cu) — ○ □ △

450 nm, Blue — △ ▲
550 nm, Green — □ ■
625 nm, Red — ○ ●

-Bulk Al reflectivity ≈ 92%
-Al(Cu) has less hillocks with annealing

Y-axis: ABSOLUTE LIGHT Reflectivity (percent) — 86, 88, 90, 92

X-axis: Annealing (1 h at each temperature) — 200°C, 350°C + 200°C, 400°C + 200°C

ARC3

I B M Confidential

After M2 (Mirror) patterning

	Wafer #42	Wafer #87
450 nm, Blue	▲	△
550 nm, Green	■	□
620 nm, Red	●	○

Bulk Al reflectivity ≅ 92%

Reflectivity (absolute %)

94
93
92
91
90
89
88
87
86

81 82 83 84 85 86

Detail of OP2

Mirror — Stud — M1 — Absorber

Detail of OP3

Mirror — Stud — M1 — Absorber

C1 (M2 no topography)   OP2   OP3
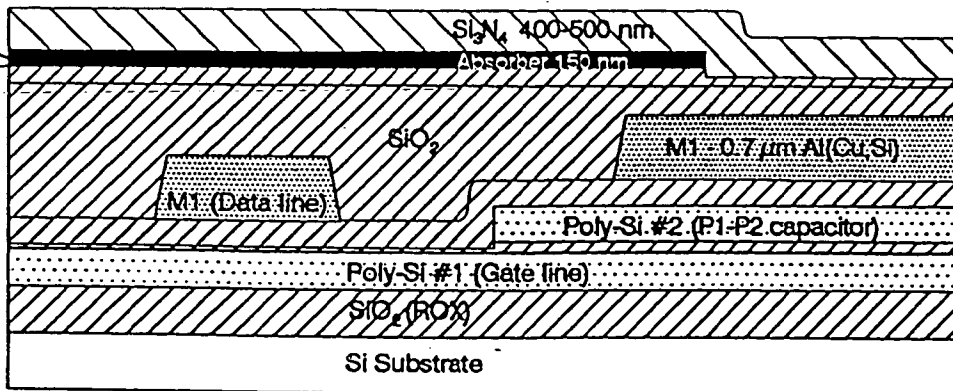
Test Structure

ARC4

LIGHT

Fig. 4

FIG 5

a) Liftoff 0.7 μm Al(Cu,Si) M1.
Deposit thick oxide.

FIG 6
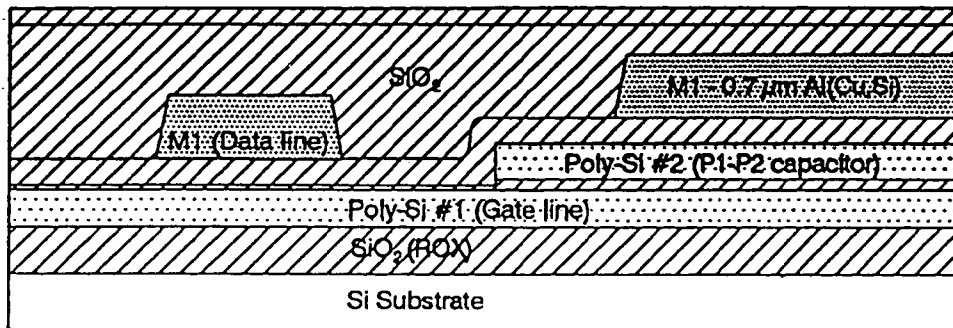
b) CMP oxide leaving 500 nm
on highest M1 point.
Deposit 200 nm oxide.

FIG 7

c) Deposit 10 nm Ti/ 100 nm
Al/ 50 nm TiN, pattern with
AR mask.
Deposit 400-500 nm nitride.

Fig. 5(a-c)

ARC5A

96

Si₃N₂ 400-500 nm

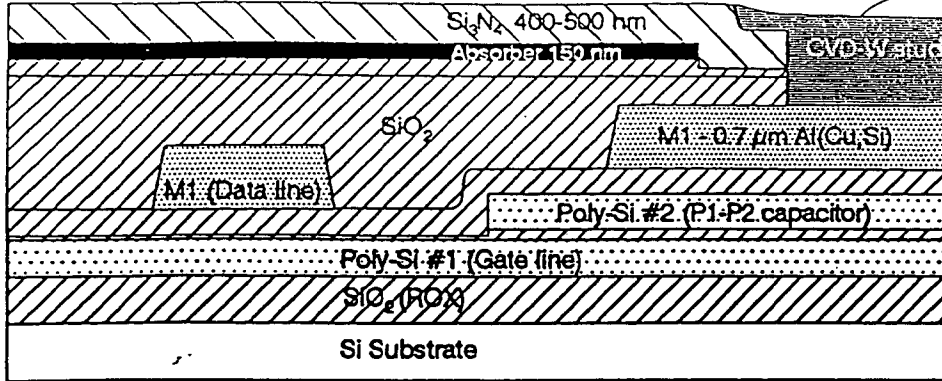Absorber 150 nm

CVD-W stud

SiO₂

M1 - 0.7 μm Al(Cu,Si)

M1 (Data line)

Poly-Si #2 (P1-P2 capacitor)

Poly-Si #1 (Gate line)

SiO₂ (ROX)

Si Substrate

FIG 8

d) Pattern with V1 mask.
Deposit liner & CVD-W.
W Chem-mech polish.

Al mirror 150 nm (M2)

1.5 μm inter-pel gap   Si₃N₄ 400-500 nm

Absorber 150 nm

CVD-W stud

SiO₂

M1 - 0.7 μm Al(Cu,Si)

M1 (Data line)

Poly-Si #2 (P1-P2 capacitor)

Poly-Si #1 (Gate line)

SiO₂ (ROX)

Si Substrate
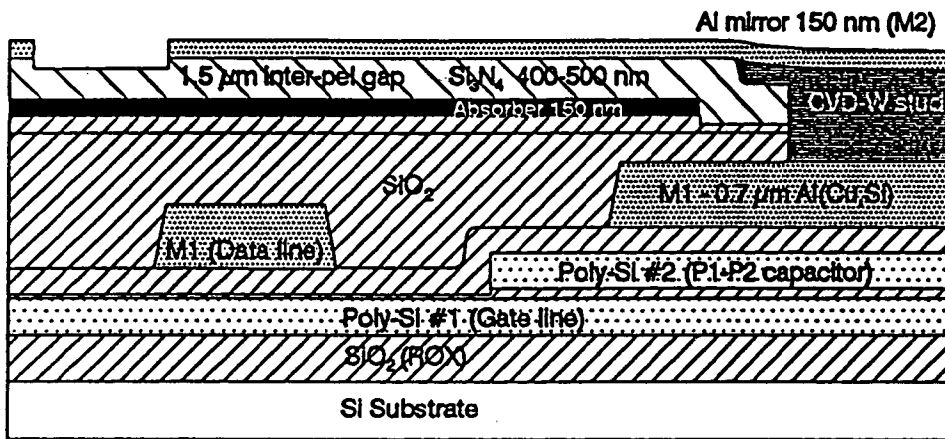
FIG 9

e) Deposit 10 nm Ti/ 150 nm
Al, pattern with M2 mask.

3.2 or 3.5 μm
SiO₂ Spacer

(M2-AR capacitor)   Al mirror 150 nm (M2)

1.5 μm inter-pel gap   Si₃N₄ 400-500 nm

Absorber 150 nm

CVD-W stud

SiO₂

M1 - 0.7 μm Al(Cu,Si)

M1 (Data line)

Poly-Si #2 (P1-P2 capacitor)

Poly-Si #1 (Gate line)

SiO₂ (ROX)

Si Substrate
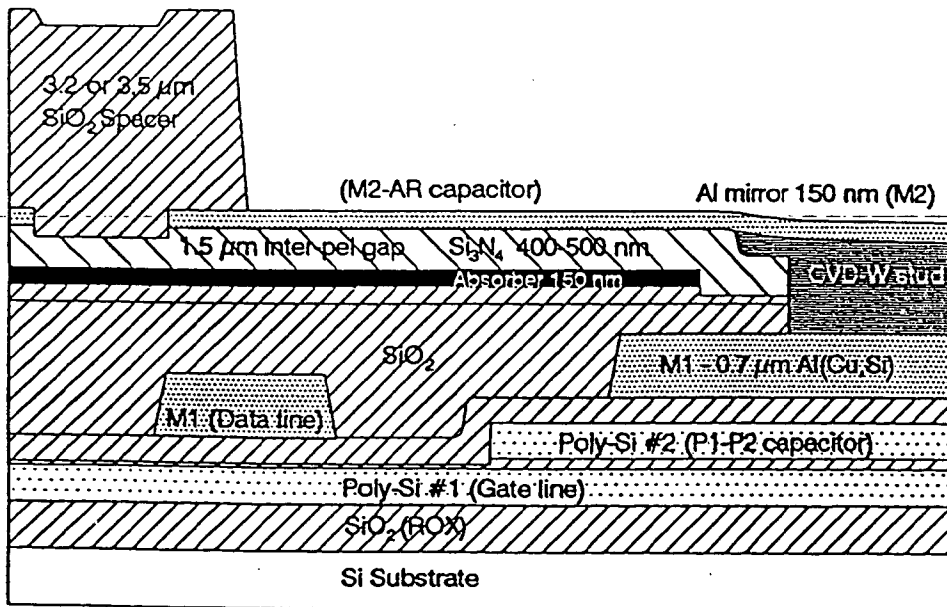
f) Deposit 2.2 or 3 μm oxide,
pattern with SP mask. Open
up M1 pads with TV mask.

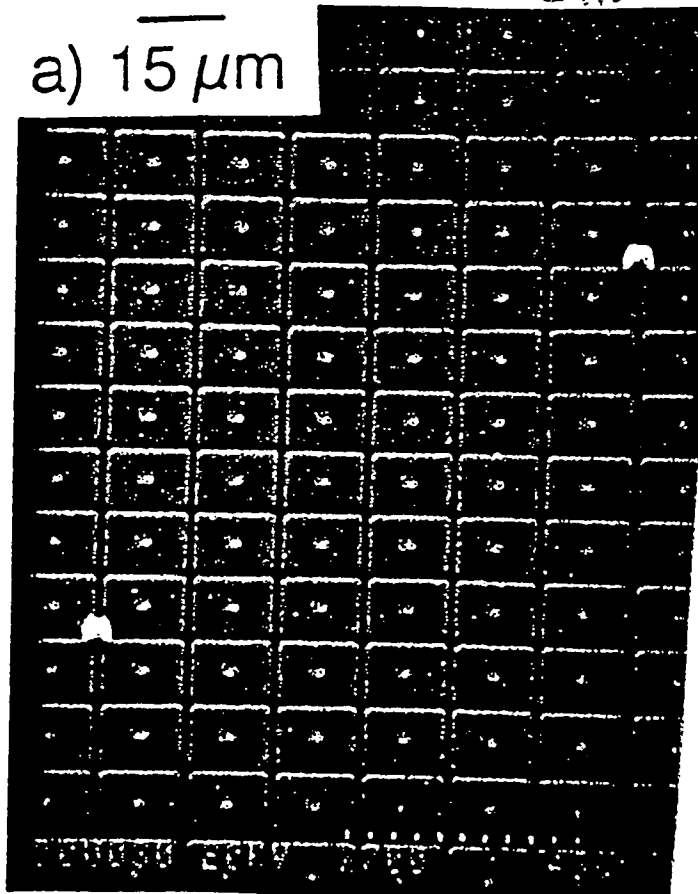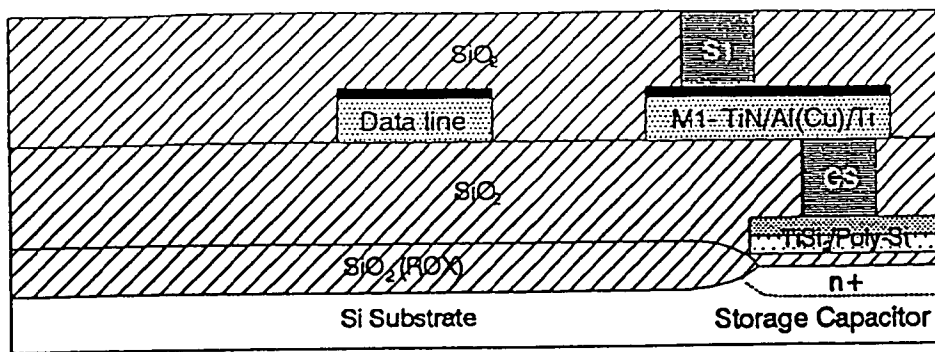Fig. 5(d-f)   FIG 10

a) 15 μm

Fig. 11

FIG. 12

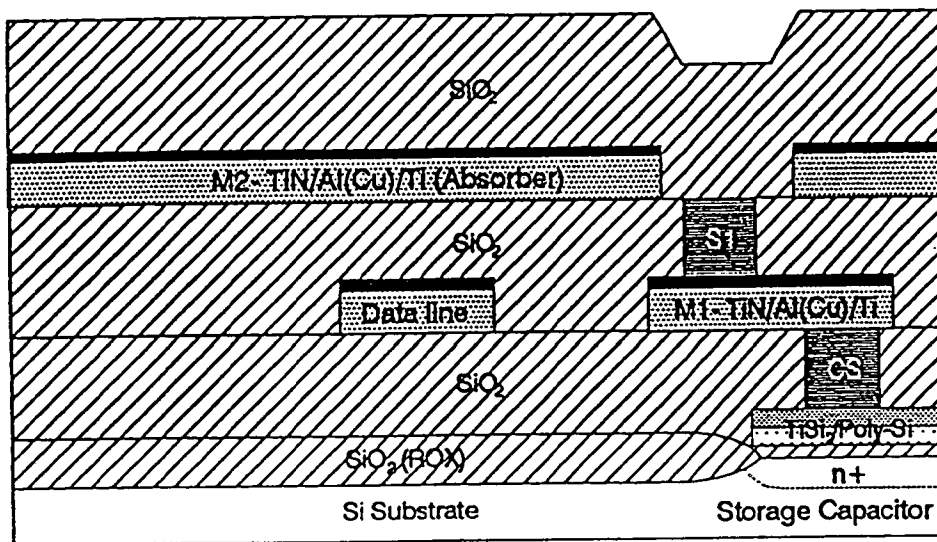a) Use standard CMOS 4 process to S1.

FIG. 13

b) Pattern POR M2 as Absorber layer. POR oxide deposition.

Fig. 8(a-c)
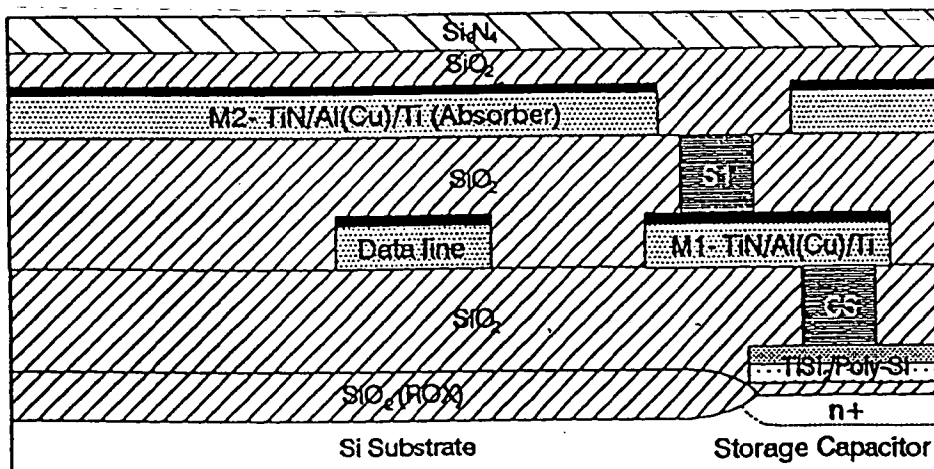
FIG. 14

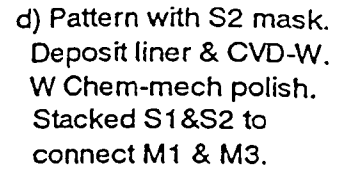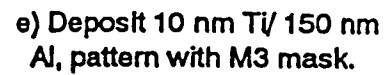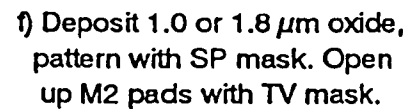c) CMP oxide leaving 500 nm on highest M2 point. Deposit 300 nm nitride.

ARC6A

FIG 15

d) Pattern with S2 mask.
   Deposit liner & CVD-W.
   W Chem-mech polish.
   Stacked S1&S2 to
   connect M1 & M3.

FIG 16

e) Deposit 10 nm Ti/ 150 nm
   Al, pattern with M3 mask.

~~Fig. 8(d-f)~~ FIG 17

f) Deposit 1.0 or 1.8 μm oxide,
   pattern with SP mask. Open
   up M2 pads with TV mask.

ARC6B